# Introduction to Automated Polyhedral Code Optimizations and Tiling

#### Alain Darte

CNRS, Compsys team Laboratoire de l'Informatique du Parallélisme École normale supérieure de Lyon

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# Outline

### Generalities

- 2 Polyhedral compilation
- Classic loop transformations
- 4 Systems of uniform recurrence equations
- 5 Detection of loop parallelism
- 6 Kernel offloading and loop tiling
- Inter-tile data reuse and local storage

# **GENERALITIES**

### Compiler: generalities



## Compiler: generalities



- AoT vs JIT
- Static vs dynamic
- Cross compilation
- Parametric codes
- Worst-case opt. vs average-case opt.
- Language-specific or multi-language
- Intermediate representations (IR)
- Runtime & libraries
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### Front-end and back-end



Figures from http://fr.slideshare.net/ssuser2cbb78/gcc-37841549.

#### Front-end

- Target independent
- Source-to-source
- High-level transf.
- Task & loop par.
- Memory opt.

#### Back-end

- Target dependent
- Instr-level par. (ILP)
- Pipelining
- AVX, SIMD instr.
- SSA and registers

### Moore's law (1965)

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- Reduction by  $\lambda$  of capacitance ( $C \sim A/\Delta$ ).
- Reduction by  $\lambda$  of voltage, intensity, and delay time  $(1/f \sim CV/I)$ .
- $P' = (C/\lambda).(V^2/\lambda^2).(\lambda f) = P/\lambda^2$  thus power density constant.
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End of Dennard scaling  $f \sim V - V_t$  (supply minus threshold voltage). But leakage power not negligible if  $V_t$  too small.

- Frequency max around 2006 ( $\sim$  4*GHz*).
- ILP, low-power CPU designs, multicore designs, GPUs.

More burden on the programmers & compilers.

#### Amdahl's law (1967)

- $T_{seq} = sT_{seq} + (1 s)T_{seq}$ , with s fraction not parallelizable.
- With p proc.,  $T_{\text{par}}/T_{\text{seq}} \ge s + (1-s)/p \ge s$ . Speed-up  $\le 1/s$ .

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Simplistic view: correct formula in wrong model ( $\sim PRAM$ ).

- Memory, comm., dedicated cores, program scaling, algorithmics!
- No insight even in favorable case, e.g., 2 independent purely sequential threads. Better: degree of parallelism, critical path, ratio comm./computation, data locality (spatial & temporal), bandwidth.
- But: make sure single core perf. remains good in parallel implem.

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Gustafson's law Different reasoning, "scaling" programs.

- $T_{\text{par}} = sT_{\text{par}} + (1 s)T_{\text{par}}$ , with s fraction of time in seq. core.
- With p proc.,  $T_{seq}/T_{par} \ge s + (1-s)p$ . Speed-up  $\ge (1-s)p$ .

Performance increase how much is due to frequency increase, architecture improvements, compilers, algorithm design?

Today's complications Multi-level parallelism, memory hierarchy, bandwidth issues, attached accelerators, evolution in programming models.

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Compiler challenges

- PPPP Programmability, performance, portability, productivity.
- Virtualization New IRs, Just-in-time (JIT) compilation, runtimes.
- Maintenance Retargetable compilers, cleaner designs.
- Predictability Architecture design, worst-case execution time (WCET).
- Certification Correct-by-construction, verification, certified compilers.
- Languages Domain-specific languages, parallel languages.

New expectations, new compiler issues, but we can solve more.
 Automatic parallelization is irrealistic, but semi-automatic tools can help.

# POLYHEDRAL COMPILATION

### One view of history (borrowed from Steven Derrien)



Some actors of this evolution are here:

P. Feautrier, P. Quinton, S. Rajopadhye, F. Irigoin, J. Ramanujam, A. Darte, A. Cohen, U. Bondhugula, S. Verdoolaege, T. Yuki, T. Grosser.

# Multi-dimensional affine representation of loops and arrays

#### Matrix Multiply



Instance-wise, element-wise, symbolic, parametric

Polyhedral Description	Omega/ISCC syntax	
Domain := [n]->{S[i,j]: 0<=i,j <n; 0<="i,j,k&lt;n};&lt;/td" t[i,j,k]:=""></n;>		
Read := $[n] \rightarrow \{T[i, j, k] \rightarrow A[i, k]\}$	]; T[i,j,k]->B[k,j]; T[i,j,k]->C[i,j]};	
Write := [n]->{S[i,j]->C[i,j]; T[i,j,k]->C[i,j]};		
Order := [n]->{S[i,j]->[i,j,0]	]; T[i,j,k]->[i,j,1,k]};	

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Polyhedral Description	Omega/ISCC syntax	So, that's it?
Domain := [n]->{S[i,j]: 0<=i,j <n; 0<="i,j,k&lt;n};&lt;/td" t[i,j,k]:=""></n;>		
<pre>Read := [n]-&gt;{T[i,j,k]-&gt;A[i,k]; T[i,j,k]-&gt;B[k,j]; T[i,j,k]-&gt;C[i,j]};</pre>		
Write := [n]->{S[i,j]->C[i,j]; T[i,j,k]->C[i,j]};		
Order := [n]->{S[i,j]->[i,j,C	); T[i,j,k]->[i,j,1,k]};	

### Ex: PPCG code for CPU+GPU, GPU part

```
__global__ void kernel0(float *A, float *B, float *C, int n) /* n=12288 */
   int b0 = blockIdx.v. b1 = blockIdx.x: /* Grid: 192x192 blocks, each with 32x32 threads */
   int t0 = threadIdx.y, t1 = threadIdx.x; /* Loops: 384x384x768 tiles, each with 32x32x16 points */
   shared float shared A[32][16]; /* Thus 1 block = 2x2x768 tiles, 1 thread = 1x1x16 points */
   __shared__ float shared_B[16][32];
   float private_C[1][1];
   for (int g1 = 32 * b0; g1 <= 12256; g1 += 6144) /* 6144 = 32 (tile size) x 192 (number of blocks) */
     for (int g3 = 32 * b1; g3 <= 12256; g3 += 6144) {
       private_C[0][0] = C[(t0 + g1) * 12288 + (t1 + g3)];
       for (int g9 = 0; g9 <= 12272; g9 += 16) { /* 16 consecutive points along k in a thread */
         if (t0 <= 15) /* 32x32 threads, only 16x32 do the transfer */
          shared B[t0][t1] = B[(t0 + g9) * 12288 + (t1 + g3)];
         if (t1 <= 15) /* 32x32 threads, only 32x16 do the transfer */
          shared A[t0][t1] = A[(t0 + g1) + 12288 + (t1 + g9)];
         syncthreads():
         for (int c4 = 0; c4 <= 15; c4 += 1) /* compute the 16 consecutive points along k */
          private C[0][0] += (shared A[t0][c4] * shared B[c4][t1]);
         __syncthreads();
       ŀ
       C[(t0 + g1) * 12288 + (t1 + g3)] = private C[0][0];
      __syncthreads();
     ŀ
3
```

PPCG compiler (Parkas) Verdoolaege, Cohen, etc.

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### Ex: PPCG code for CPU+GPU, GPU part (Volkov-like)

```
__global__ void kernel0(float *A, float *B, float *C, int n) /* n=12288 */
   int b0 = blockIdx.v. b1 = blockIdx.x: /* Grid: 192x192 blocks, each with 16x16 threads */
   int t0 = threadIdx.y, t1 = threadIdx.x; /* Loops: 384x384x768 tiles, each with 32x32x16 points */
   shared float shared A[32][16]; /* Thus 1 block = 2x2x768 tiles, 1 thread = 2x2x16 points */
   shared float shared B[16][32]:
   float private_C[2][2];
   for (int g1 = 32 * b0; g1 <= 12256; g1 += 6144) /* 6144 = 32 (tile size) x 192 (number of blocks) */
     for (int g3 = 32 * b1; g3 <= 12256; g3 += 6144) {
       private C[0][0] = C[(t0 + g1) * 12288 + (t1 + g3)]; /* 2x2 points unrolled for register usage */
       private C[0][1] = C[(t0 + g1) * 12288 + (t1 + g3 + 16)];
       private C[1][0] = C[(t0 + g1 + 16) * 12288 + (t1 + g3)];
       private C[1][1] = C[(t0 + g1 + 16) * 12288 + (t1 + g3 + 16)];
       for (int g9 = 0; g9 <= 12272; g9 += 16) { /* 16 consecutive points along k in a thread */
        for (int c1 = t1: c1 <= 31: c1 += 16) /* 16x32 to bring with 16x16 threads */
          shared B[t0][c1] = B[(t0 + g9) * 12288 + (g3 + c1)];
        for (int c0 = t0; c0 <= 31; c0 += 16) /* 32x16 to bring with 16x16 threads */
          shared A[c0][t1] = A[(g1 + c0) * 12288 + (t1 + g9)];
        __syncthreads();
        for (int c2 = 0; c2 <= 15; c2 += 1) { /* unrolled for register usage */
          private_C[0][0] += (shared_A[t0][c2] * shared_B[c2][t1]);
          private_C[0][1] += (shared_A[t0][c2] * shared_B[c2][t1 + 16]);
          private C[1][0] += (shared A[t0 + 16][c2] * shared B[c2][t1]);
          private C[1][1] += (shared A[t0 + 16][c2] * shared B[c2][t1 + 16]);
         3
        __syncthreads();
       ŀ
       C[(t0 + g1) * 12288 + (t1 + g3)] = private C[0][0]:
                                                                             PPCG compiler (Parkas)
       C[(t0 + g1) * 12288 + (t1 + g3 + 16)] = private C[0][1]:
                                                                             Verdoolaege, Cohen, etc.
       C[(t0 + g1 + 16) * 12288 + (t1 + g3)] = private_C[1][0];
       C[(t0 + g1 + 16) * 12288 + (t1 + g3 + 16)] = private C[1][1];
                                                                      イロト イボト イヨト イヨト
       __syncthreads();
                                                                                                      12/98
     3
```

# Typical criticism against polyhedral techniques

Too hard to understand

Heavy formalism

No such codes

Not worth the effort

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Key to reason on multi-dimensional computations and data structures, and avoid explicit unrolling. More applications to come (e.g., loop termination, parallel languages, verification/certification, WCET).

# (Parametric) analysis, transformations, optimizations

#### Loop transformations

- Automatic parallelization.
- Transformations framework.
- Scanning & code generation.
- Dynamic & speculative opt.

#### Mapping computations & data

- Systolic arrays design.
- Data distribution.
- Communication opt.
- Streams optimizations.

#### and many more...

#### Instance/element-wise analysis

- Single assignment.
- Liveness, array expansion/reuse.
- Analysis of parallel programs.
- Data races & deadlocks detection.

### Counting, (de-)linearizing

- Cache misses.
- FIFOs, array linearizations.
- Memory size computations.
- Loop termination (e.g., WCET).

#### Tools

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- ✓ PIP: parametric (I)LP.
- ✓ Polylib: polyhedra, generators.
- ✓ Omega, isl/iscc: integer sets, Presburger.
- ✓ Ehrhart & Barvinok: counting.
- ✓ Cloog: code generation.
- ✓ Fada/Candl: dataflow analysis.
- Cl@k: critical lattices and array contraction.
- Clan: polyhedral "extractor".Clint: visualization.

### Compiler or infrastructures

- ✓ Alpha: SAREs to HLS.
- ✓ Compaan: polyhedral streams.
- ✓ Pips, Par4All, dHPF, Pluto,
   & R-Stream: parallelizing compilers.
- ✓ Graphite: library for GCC.
- ✓ Polly: library for LLVM.
- ✓ Gecos: user-friendly tool for HLS.
- ✓ PiCo, Chuba, PolyOpt: HLS compilers/prototypes.
- ✓ PPCG: code generator for GPU.
- ✓ Apollo: static/dynamic opt.

. . .

# Basic form: affine bounds and array access functions

#### Fortran DO loops:

Affine bounds of surrounding counters & parameters.

- Multi-dimensional arrays, same restriction for access functions.
- Loop increment = 1.
- Iteration domain: polyhedron.
- Iteration vector (*i*, *j*).
- Lexico. order:  $S(i,j) \rightarrow (i,j,0)$ ,  $T(i,j) \rightarrow (i,j,1)$ .

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**DO loops**: few lines for a (possibly) large set of regular computations.

- Smaller code size.
- Repetitive structure: regularity that can be exploited.
- Hot parts of codes where optimizations are needed.
- Large potential for optimizations (e.g., parallelism, memory usage).
- Algorithms complexity depends on code size, not computations size.
- Parametric loops, needed for "optimality" w.r.t. unroll version.
- Abstraction between low-level (hardware) & high-level (program).

Arrays: similar properties for multi-dimensional storage.

To be exploited: structure, parameters, symbolic unrolling.

### Be careful: different types of codes with loops

#### Fortran DO loops:

```
DO i=1, N

DO j=1, N

a(i,j) = c(i,j-1)

c(i,j) = a(i,j) + a(i-1,N)

ENDDO

ENDDO
```

```
C for and while loops:
y = 0; x = 0;
while (x <= N && y <= N) {
    if (?) {
        x=x+1;
        if (y >= 0 && ?) y=y-1;
    }
    y=y+1;
}
```

#### C for loops:

```
for (i=1; i<=N; i++) {
  for (j=1; j<=N; j++) {
    a[i][j] = c[i][j-1];
    c[i][j] = a[i][j] + a[i-1][N];
  }
}</pre>
```

#### Uniform recurrence equations

```
\forall (i,j) \text{ such that } 1 \leq i,j \leq N
```

$$\begin{cases} a(i,j) = c(i,j-1) \\ b(i,j) = a(i-1,j) + b(i,j+1) \\ c(i,j) = a(i,j) + b(i,j) \end{cases}$$

### More types of codes with loops

#### FAUST: real-time for music

```
random = +(12345) ~ *(1103515245);
noise = random/2147483647.0;
process = random/2 : @(10);
```

```
\Leftrightarrow \left\{ \begin{array}{l} R(t) = 12345 + 1103515245 \times R(t-1) \\ N(t) = R(t)/2147483647.0; \\ P(t) = 0.5 \times R(t-10) \end{array} \right.
```

#### Array languages

```
A = B + C
A[1:n] = A[0:n-1] + A[2:n+1]
```

#### OpenStream

```
#pragma omp task output (x) // Task T1
x = ...;
for (i = 0; i < N; ++i) {
    int window_a[2], window_b[3];
    #pragma omp task output (x < window_a[2]) // Task T2
    window_a[0] = ...; window_a[1] = ...;
    if (i % 2) {
        #pragma omp task input (x > window_b[2]) // Task T3
        use (window_b[0], window_b[1]);
    }
    #pragma omp task input (x) // Task T4
    use (x);
}
```

#### X10 parallel language

finish
 for (i in 0..n-1){
 S1;
 async S2;
 }



Linear programming, integer linear programming, parametric optimization minlex{ $x \mid Ax \ge Bn + c, x \ge 0$ }

### Some fundamental mathematical tools

Linear programming, integer linear programming, parametric optimization minlex{ $x \mid Ax \ge Bn + c, x \ge 0$ }

If non-empty sets, duality theorem  $\min\{c.x \mid Ax \ge b, x \ge 0\} = \max\{y.b \mid yA \le c, y \ge 0\}$
Linear programming, integer linear programming, parametric optimization minlex{ $x \mid Ax \ge Bn + c, x \ge 0$ }

If non-empty sets, duality theorem and affine form of Farkas lemma  $\min\{c.x \mid Ax \ge b, x \ge 0\} = \max\{y.b \mid yA \le c, y \ge 0\}$  $c.x \le d \quad \forall x \text{ s.t. } Ax \le b \Leftrightarrow \exists y \ge 0 \text{ s.t. } c = yA \text{ and } y.b \le d$ 

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Lattices, systems of Diophantine equations, Hermite and Smith forms Lattice:  $\mathcal{L} = \{x \mid \exists y \in \mathbb{Z}^n \text{ s.t. } x = Ay\}$ Hermite: A = QH, Q unimodular, H triangular. Smith:  $A = Q_1SQ_2$ ,  $Q_1$  and  $Q_2$  unimodular, and S diagonal.

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Manipulation of integer sets, Presburger arithmetic, counting

Chernikova, Ehrhart, Barvinok, quasi-polynomials

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Manipulation of integer sets, Presburger arithmetic, counting

Chernikova, Ehrhart, Barvinok, quasi-polynomials

In many cases, no need to really understand the theory anymore 🖝 ISL

# $\min\{c.x \mid Ax \ge b, x \ge 0\} = \max\{y.b \mid yA \le c, y \ge 0\}$

$$\min \begin{cases} 11t + 10u \mid \\ 2t + 3u \ge 5 \\ 3t + 2u \ge 4 \\ 5t + u \ge 12 \\ t \ge 0, \ u \ge 0 \end{cases} = \max \begin{cases} 5x + 4y + 12z \mid \\ 2x + 3y + 5z \le 11 \\ 3x + 2y + z \le 10 \\ x \ge 0, \ y \ge 0, \ z \ge 0 \end{cases}$$

Primal problem: doped athlete buy the right numbers t and u of doping pills (with unit price 11 and 10) to get a sufficient intake (5, 4, and 12) of 3 elementary products, knowing the content of each mixed product. Dual problem: dealer sell the 3 elementary products at maximal price, while being cheaper than doping pills.

# $\min\{c.x \mid Ax \ge b, x \ge 0\} = \max\{y.b \mid yA \le c, y \ge 0\}$

$$\min \left\{ \begin{array}{ll} 11t + 10u \mid \\ 2t + 3u \ge 5 \\ 3t + 2u \ge 4 \\ 5t + u \ge 12 \\ t \ge 0, \ u \ge 0 \end{array} \right. = \max \left\{ \begin{array}{ll} 5x + 4y + 12z \mid \\ 2x + 3y + 5z \le 11 \\ 3x + 2y + z \le 10 \\ x \ge 0, \ y \ge 0, \ z \ge 0 \end{array} \right.$$

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Complexity

- Optimal rational solution: polynomial (L. Khachiyan).
- Optimal integer solution: NP-complete and inequality only.
- Simplex algorithm (fast in practice), basis reduction (Lenstra et al.), parametric linear programming (P. Feautrier).

### Example of Sven Verdoolaege's iscc script

See tutorial http://barvinok.gforge.inria.fr/tutorial.pdf. Example borrowed from http://compsys-tools.ens-lyon.fr/iscc/ (thanks to A. Isoard).

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```
# void polynomial_product(int n, int *A, int *B, int *C) {
      for(int k = 0: k < 2*n-1: k++)
#
# S:
      C[k] = 0;
     for(int i = 0; i < n; i++)</pre>
#
# for(int j = 0; j < n; j++)</pre>
               C[i+i] += A[i] * B[i]:
# T:
# }
Domain := [n] \rightarrow \{
    S[k] : k <= -2 + 2n and k >= 0:
    T[i, j] : i \ge 0 and i \le -1 + n and j \le -1 + n and j \ge 0;
};
Read := [n] -> \{
    T[i, j] \rightarrow C[i + j]; T[i, j] \rightarrow B[j]; T[i, j] \rightarrow A[i];
} * Domain:
Write := [n] -> {
    S[k] \rightarrow C[k]; T[i, j] \rightarrow C[i + j];
} * Domain;
Schedule := [n] \rightarrow f
    T[i, j] \rightarrow [1, i, j]; S[k] \rightarrow [0, k, 0];
};
                                                                 ▲□▶ ▲□▶ ▲ヨ▶ ▲ヨ▶ ヨー つくで
```

### Example of Sven Verdoolaege's iscc script (Cont'd)

```
Schedule := [n] -> {
    T[i, j] -> [1, i, j]; S[k] -> [0, k, 0];
};
```

We get the strict sequential order of operations in the program:

print RaW;

We get the read-after-write memory-based data dependences:

### Some iscc features and syntax with sets and relations/maps

+, -, \* union, difference, intersection. domain m, range m set from map. m(s) apply map to set. m1.m2 join of maps.

- s1 cross s2, m1 cross m2 cartesian product. deltas m set of differences.
- coefficients s constraints for Farkas lemma.

lexmin s, lexmin m lexicographic minimum, same for max.

codegen s, codegen m scanning domain (following map m). Example: codegen RaW;

```
for (int c0 = 0; c0 < n; c0 += 1)
for (int c1 = 0; c1 < n; c1 += 1) {
  for (int c2 = max(0, -n + c0 + c1 + 1); c2 < c0; c2 += 1)
      T(c2, c0 + c1 - c2);
    S(c0 + c1);
}</pre>
```

card s, card m Number of integer points in set or image. Example: print card RaW;

```
[n] → { S[k] → ((-1 + 2 * n) - k) : n <= k <= -2 + 2n;
S[k] → (1 + k) : 0 <= k < n;
T[i, j] → ((-1 + n) - i) : i <= -2 + n and n - i <= j < n;
T[i, j] → j : i >= 0 and 0 < j < n - i }</pre>
```

### Courses in 2013 polyhedral spring school

See the thematic quarter on compilation http://labexcompilation.ens-lyon.fr/ for polyhedral spring school and keynotes on HPC languages.

- S. Rajopadhye A view on history.
- P. Feautrier "Basics" in terms of mathematical concepts.
- L.-N. Pouchet Polyhedral loop transformations, scheduling.
- S. Verdoolaege Integer sets & relations: high-level modeling and implem.
- A. Miné Program invariants and abstract interpretation.
- B. Creusillet Array region analysis and applications.
- U. Bondhugula (+ A. Darte) Compil. for distr. memory, memory mapping. Sadayappan (+ N. Vasilache) Polyhedral transf. for SIMD architectures.

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Missing topics: tiling, dependence analysis, induction variable recognition, array privatization, loop fusion, code generation, Ehrhart theory, locality optimizations, benchmarks, high-level synthesis, trace analysis, program equivalence, termination, extensions, pipelining, streams/offloading, ...

# CLASSIC LOOP TRANSFORMATIONS

Loop unrolling (by constant factor) Software pipelining Loop fusion/distribution Loop peeling/statement sinking loop shifting (retiming) Loop interchange Loop skewing (by constant factor) Loop reversal Unimodular transformation Affine transformation

Strip mining (by parametric factor) Unroll-and-jam Loop tiling Scalar privatization/expansion Single assignment expansion Array unrolling Array padding Array linearization Array contraction Affine modulo allocation

$$\begin{array}{l} \text{DO i=1, 10} \\ \text{a(i)} = \text{b(i)} \\ \text{d(i)} = \text{a(i-1)} \\ \text{ENDDO} \end{array}$$

Unrolling by 2

$$\begin{array}{l} \text{DO i=1, 10, 2} \\ \text{a(i)} = \text{b(i)} \\ \text{d(i)} = \text{a(i-1)} \\ \text{a(i+1)} = \text{b(i+1)} \\ \text{d(i+1)} = \text{a(i)} \\ \text{ENDDO} \end{array}$$

#### Partial unrolling

- Replicates instructions to improve schedule & resource usage.
- Can be used for array scalarization.
- Increases code size and (indirectly) register usage.

#### Total loop unrolling

• Flattens the loops and changes structure.

# Strip mining, loop coalescing



Loop linearization

DO  $I_s=1$ , N, s DO  $i=I_s$ , min(N,  $I_s+s-1$ ) a(i) = b(i) + c(i)ENDDO ENDDO

#### Strip mining

- Performs parametric loop unrolling.
- Changes the structure (2D space).
- Creates blocks of computations.
- Can be used as a preliminary step for tiling.

#### Loop linearization

- Can reduce the control of loops.
- Reduces the problem dimension.

Optimize throughput, with dependence & resource constraints. Cyclic dependence graph with iteration distance (+ latency information).



Optimize throughput, with dependence & resource constraints. Cyclic dependence graph with iteration distance (+ latency information).

	e compaction
L400:       L400: $Id[r26] \rightarrow r27$ $Id[r26] \rightarrow r27$ nop       nop         add r27, 6740 $\rightarrow$ r26       add r27, 6740 $\rightarrow$ r26 $Id 0x1A54[r27] \rightarrow r27$ $Id 0x1A54[r27] \rightarrow r27$ nop       nop         sub.f r27, r25 $\rightarrow$ r0       sub.f r27, r25 $\rightarrow$ r0         bne L400       bne L400         nop       nop         sub.f v27, r25 $\rightarrow$ r0       sub.f r27, r25 $\rightarrow$ r0         bne L400       bne L400         nop       nop         sub.f v27, r25 $\rightarrow$ r0       0,1         E       E	): $[r26] \rightarrow r27$ nop $Id r27, 6740 \rightarrow r26$ $0x1A54[r27] \rightarrow r27$ nop $ib.f r27, r25 \rightarrow r0$ nop 0.2 0.1 0.2 0.1 0.2 0.1 0.2 0.1 0.2 0.2 0.1 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.1 0.2

Optimize throughput, with dependence & resource constraints. Cyclic dependence graph with iteration distance (+ latency information).

Sequential code	Code compaction	A
L400: $ld[r26] \rightarrow r27$ nop add r27, 6740 $\rightarrow$ r26 $ld 0x1A54[r27] \rightarrow r27$	L400: Id[r26]→ r27 nop Id 0×1A54[r27]→ r27 add r27, 6740→ r26	
nop sub.f r27, r25 → r0 bne L400 nop	nop sub.f r27, r25→ r0 bne L400 nop	
L399: <mark>8</mark> n cycles.	L399:	0,1 E

Optimize throughput, with dependence & resource constraints. Cyclic dependence graph with iteration distance (+ latency information).

Sequential code	Code compaction	A
L400: $ld[r26] \rightarrow r27$ nop add r27, 6740 $\rightarrow$ r26 $ld 0x1A54[r27] \rightarrow r27$ nop sub.f r27, r25 $\rightarrow$ r0 bne L400 nop L399:	L400: $Id[r26] \rightarrow r27$ nop $Id 0x1A54[r27] \rightarrow r27$ $add r27, 6740 \rightarrow r26$ $sub.f r27, r25 \rightarrow r0$ bne L400 nop L399:	0,2 0,2 0,2 0,1 0,1 0,1 0,1 0,1
8n cycles.	7 <i>n</i> cycles.	E

Optimize throughput, with dependence & resource constraints. Cyclic dependence graph with iteration distance (+ latency information).



Optimize throughput, with dependence & resource constraints. Cyclic dependence graph with iteration distance (+ latency information).



Optimize throughput, with dependence & resource constraints. Cyclic dependence graph with iteration distance (+ latency information).



Optimize throughput, with dependence & resource constraints. Cyclic dependence graph with iteration distance (+ latency information).

Ex: sequential, pipelined LANai3.0, load & branch = one "shadow".

Sequential code	Code compaction	Software pipelining $+$ speculation
L400: $H[r_{26}] \rightarrow r_{27}$	L400: $Id[r_{26}] \rightarrow r_{27}$	$ld[r26] \rightarrow r27$
nop	nop	add r27, 6740 $\rightarrow$ r26
add r27, 6740 $\rightarrow$ r26 Id 0x1A54[r27] $\rightarrow$ r27	ld 0x1A54[r27] $\rightarrow$ r27 add r27. 6740 $\rightarrow$ r26	L400: Id 0×1A54[r27]→ r27
nop	<b>sub.f</b> r27, r25 $\rightarrow$ r0	$Id[r26] \rightarrow r27$
sub.t r27, r25 $\rightarrow$ r0 bne L400	bne L400 nop	sub.t r27, r25 $\rightarrow$ r0 bne L400
nop I 399·	L399:	add r27, 6740 $\rightarrow$ r26
8 <i>n</i> cycles.	7n cycles.	3 + 5n cycles.

 $\sigma(S, i) = \lambda . i + \rho_S = \lambda . (i + q_S) + r_S \text{ with } 0 \le r_S < \lambda \text{ i.e., } r_S = \rho_S \text{ mod } \lambda$  $\Rightarrow \text{ Modulo scheduling: initiation interval (1/throughput). Here } \lambda = 5.$ 

# Loop shifting or retiming

 $\begin{array}{ccc} \text{DO } i=1, \text{ N} & & \text{IF} \\ a(i) = b(i) & & \text{Loop shifting} \\ d(i) = a(i-1) & & \longleftrightarrow & & \text{IF} \\ \text{ENDDO} & & & & & \text{IF} \end{array}$ 

DO i=0, N IF (i > 0) THEN a(i) = b(i)IF (i < N) THEN d(i+1) = a(i)ENDDO

Here: dependence at distance 1 (loop-carried or inter-iteration) transformed into dependence at distance 0 (loop-independent or intra-iteration).

#### Main features

- Similar to software pipelining.
- Creates prelude/postlude or introduces if statements.
- Can be used to align accesses and enable loop fusion.
- Particularly suitable to handle constant dependence distances.

# Loop peeling and statement sinking

```
\begin{array}{cccc} \text{DO i=0, N} \\ \text{IF } (i > 0) \text{ THEN} \\ a(i) = b(i) & & \rightarrow \\ \text{IF } (i < N) \text{ THEN} & & \leftarrow \\ d(i+1) = a(i) & & \text{Statement sinking} \\ \text{ENDDO} \end{array}
```

#### Loop peeling

- Removes a few iterations to make code simpler.
- May enable more transformations.
- Reduces the iteration domain (range of loop counter).

#### Statement sinking

• Used to make loops perfectly nested.

# Loop distribution and loop fusion



Here: intra-loop dependence transformed into inter-loop dependence.

#### Loop distribution

- Used to parallelize/vectorize loops (no inter-iteration dependence).
- Valid if statements not involved in a circuit of dependences.
- Parallelization: separate strongly connected components.

Loop fusion

- Increases the granularity of computations.
- Reduces loop overhead.
- Usually improves spatial & temporal data locality.
- May enable array scalarization.

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### Loop parallelization with loop distribution

$$\begin{array}{l} \text{DO i=1,N} \\ \text{A(i)} &= 2*\text{A(i)} + 1 \\ \text{B(i)} &= \text{C(i-1)} + \text{A(i)} \\ \text{C(i)} &= \text{C(i-1)} + \text{G(i)} \\ \text{D(i)} &= \text{D(i-1)} + \text{A(i)} + \text{C(i-1)} \\ \text{E(i)} &= \text{E(i-1)} + \text{B(i)} \\ \text{F(i)} &= \text{D(i)} + \text{B(i-1)} \\ \text{ENDDO} \end{array}$$



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### Loop parallelization with loop distribution

```
DOPAR i=1.N
  A(i) = 2*A(i) + 1
ENDDOPAR
DOSEQ i=1,N
  C(i) = C(i-1) + G(i)
ENDDOSEQ
DOPAR i=1,N
  \mathsf{B}(\mathsf{i}) = \mathsf{C}(\mathsf{i}\text{-}1) + \mathsf{A}(\mathsf{i})
ENDDOPAR
DOSEQ i=1,N
  E(i) = E(i-1) + B(i)
ENDDOSEQ
DOSEQ i=1,N
  D(i) = D(i-1) + A(i) + C(i-1)
ENDDOSEQ
DOPAR i=1,N
  F(i) = D(i) + B(i-1)
ENDDOPAR
```



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### Loop parallelization with partial loop distribution

DOSEQ i=1,N C(i) = C(i-1) + G(i)**ENDDOSEQ** DOPAR i=1,N A(i) = 2\*A(i) + 1B(i) = C(i-1) + A(i)**FNDDOPAR** DOSEQ i=1,N D(i) = D(i-1) + A(i) + C(i-1)E(i) = E(i-1) + B(i)**ENDDOSEQ** DOPAR i=1.N F(i) = D(i) + B(i-1)**ENDDOPAR** 



Instance of typed loop fusion, with 2 types (par. & seq.), and possibly fusion-preventing edges for 1 type (par.). 

NP-complete.

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# Loop shifting and loop parallelization

Maximal typed fusion Easy for 1 type, NP-complete for  $\geq$  2 types.



$$\begin{array}{l} \text{DOPAR i=2, n} \\ a(i) = f(i) \\ b(i) = g(i) \\ \text{ENDDOPAR} i=2, n \\ c(i) = a(i-1) + b(i) \\ d(i) = a(i) + b(i-1) \\ \text{ENDDOPAR} i=2, n \\ \text{DOPAR i=2, n} \\ e(i) = d(i-1) + d(i) \\ \text{ENDDO} \end{array}$$

#### Same problem with loop shifting?

$$\begin{array}{l} \text{DO i=2, n} \\ a(i) = f(i) \\ b(i) = g(i) \\ c(i) = a(i{\text{-}}1) + b(i \\ d(i) = a(i) + b(i{\text{-}}1) \\ e(i) = d(i{\text{-}}1) + d(i \\ \text{ENDDO} \end{array}$$



$$\begin{array}{l} \text{DOPAR i=2, n} \\ a(i) = f(i) \\ b(i) = g(i) \\ \text{ENDDOPAR} \\ \text{DOPAR i=2, n} \\ c(i) = a(i-1) + b(i) \\ d(i) = a(i) + b(i-1) \\ \text{ENDDOPAR} \\ \text{DOPAR i=2, n} \\ e(i) = d(i-1) + d(i) \\ \text{ENDDO} \end{array}$$

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# Loop shifting and loop parallelization

Maximal typed fusion Easy for 1 type, NP-complete for  $\geq$  2 types.



Same problem with loop shifting? NP-complete even for 1 type.

 $\begin{array}{l} \text{DO i=2, n} \\ a(i) = f(i) \\ b(i) = g(i) \\ c(i) = a(i{\text{-}}1) + b(i) \\ d(i) = a(i) + b(i{\text{-}}1) \\ e(i) = d(i{\text{-}}1) + d(i) \\ \text{ENDDO} \end{array}$ 



 $\begin{array}{l} a(2) = f(2) \\ d(2) = a(2) + b(1) \\ \text{DOPAR i=3, n} \\ a(i) = f(i) \\ b(i-1) = g(i-1) \\ d(i) = a(i) + b(i-1) \\ \text{ENDDOPAR} \\ b(n) = g(n) \\ \text{DOPAR i=2, n} \\ c(i) = a(i-1) + b(i) \\ e(i) = d(i-1) + d(i) \\ \text{ENDDOPAR} \end{array}$ 

#### In dimension one

- Maximal fusion with shifting: NP-complete (previous slide).
- Complete fusion? Easy. Iff all (undirected) cycles have weight 0.

#### In dimension two

• Find an outer shift to enable the complete inner fusion.



DO i=1, n-1  
DOPAR j=1, n-1  

$$a(i,j) = b(i-1,j-1)$$
  
ENDDOPAR  
DOPAR j=1, n-1  
 $b(i,j) = a(i,j) + a(i,j-1)$   
ENDDOPAR  
ENDDO

#### In dimension one

- Maximal fusion with shifting: NP-complete (previous slide).
- Complete fusion? Easy. Iff all (undirected) cycles have weight 0.

#### In dimension two

• Find an outer shift to enable the complete inner fusion.



#### In dimension one

- Maximal fusion with shifting: NP-complete (previous slide).
- Complete fusion? Easy. Iff all (undirected) cycles have weight 0.

#### In dimension two

- Find an outer shift to enable the complete inner fusion.
- NP-complete (as many other retiming problems).



DO i=1, n  
DOPAR j=1, n  
IF (i>1) and (j>1) THEN  

$$b(i-1,j-1) = a(i-1,j-1) + a(i-1,j-2)$$
  
IF (i
 $a(i,j) = b(i-1,j-1)$   
ENDDOPAR  
ENDDO

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These are very particular problems & instances, but still, this shows the difficulty to "push" dependences inside, i.e., to optimize locality.

Is there some loop parallelism (i.e., parallel loop iterations) in the following two codes? What is their degree of parallelism?

```
DO i=1, N

DO j=1, N

a(i,j) = c(i,j-1)

c(i,j) = a(i,j) + a(i-1,N)

ENDDO

ENDDO

ENDDO

DO i=1, N

DO j=1, N

a(i,j) = c(i,j-1)

c(i,j) + a(i-1,j)

ENDDO

ENDDO

ENDDO
```

Is there some loop parallelism (i.e., parallel loop iterations) in the following two codes? What is their degree of parallelism?

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Loop interchange:  $(i, j) \mapsto (j, i)$ .

$$\begin{array}{ccccc} \text{DO $i=1$, $N$} & \text{Loop interchange} & \text{DO $j=1$, $N$} \\ \text{DO $j=1$, $i$} & \longleftrightarrow & \text{DO $i=j$, $N$} \\ \text{a}(i,j+1) = \text{a}(i,j) + 1 & \text{a}(i,j+1) = \text{a}(i,j) + 1 \\ \text{ENDDO} & \text{ENDDO} \\ \text{ENDDO} & \text{ENDDO} \end{array}$$

Here: dependence distance (0,1) transformed into distance (1,0).

Main features

- May involve bounds computations as in
- Can impact loop parallelism.
- Basis of loop tiling.
- Changes order of memory accesses and thus data locality.

$$\sum_{i=1}^{n} \sum_{j=1}^{i} S_{i,j} = \sum_{j=1}^{n} \sum_{i=j}^{n} S_{i,j}.$$

Interests:

- Combines outer loop unrolling and loop fusion.
- Changes order of iterations and locality, keeping same loop nesting.
- Can be viewed as a restricted form of tiling  $s \times 1$ .

## Loop reversal and loop skewing

Loop reversal:  $i \mapsto -i$ , loop executed in opposite order.

Loop skewing:  $(i, j) \mapsto (i, j + i)$ , loop iterations in the same order.



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## Unimodular transf.: reversal + skewing + interchange



Here,  $(i,j) \mapsto (t,p) = (i+j,i)$ . Loop bounds with Fourier-Motzkin elim.:

$$1 \leq i,j \leq N \Leftrightarrow 1 \leq p, t-p \leq N \Leftrightarrow 1 \leq p \leq N, t-N \leq p \leq t-1$$
  
Elimination of  $p \Rightarrow 2 \leq t \leq 2N, 1 \leq N$ , Elimination of  $t \Rightarrow 1 \leq N$ 

## Unimodular transf.: reversal + skewing + interchange

Here,  $(i,j) \mapsto (t,p) = (i+j,i)$ . Loop bounds with Fourier-Motzkin elim.:

$$1 \leq i,j \leq N \Leftrightarrow 1 \leq p, t-p \leq N \Leftrightarrow 1 \leq p \leq N, t-N \leq p \leq t-1$$
  
Elimination of  $p \Rightarrow 2 \leq t \leq 2N, 1 \leq N$ , Elimination of  $t \Rightarrow 1 \leq N$ 

In general: "For all  $\vec{i} \in \mathcal{P}$  do  $S(\vec{i})$ "  $\longrightarrow$  "For all  $\vec{p} \in U\mathcal{P}$  do  $S(U^{-1}\vec{p})$ ".

$$\left(\begin{array}{c}t\\p\end{array}\right) = U\left(\begin{array}{c}i\\j\end{array}\right) \quad \left(\begin{array}{c}i\\j\end{array}\right) = U^{-1}\left(\begin{array}{c}t\\p\end{array}\right) \quad \text{Here} \quad U = \left(\begin{array}{c}1&1\\1&0\end{array}\right) \quad U^{-1} = \left(\begin{array}{c}0&1\\1&-1\end{array}\right)$$

New implicit execution order: iterate lexicographically on (t, p). If  $S(\vec{i})$  depends on  $T(\vec{j})$ , dep. distance  $d = \vec{i} - \vec{j}$  lexico-positive:  $\vec{d} \succeq_{\text{lex}} \vec{0}$ . New distance  $\vec{d'} = U(\vec{i} - \vec{j}) = U\vec{d}$ . Validity condition:  $\vec{d'} = U\vec{d} \succeq_{\text{lex}} \vec{0}$ .

## Loop tiling, blocked algorithms



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## In practice, need to combine all. Ex: HLS with C2H Altera

Optimize DDR accesses for bandwidth-bound accelerators.

- Use tiling for data reuse and to enable burst communication.
- Use fine-grain software pipelining to pipeline DDR requests.
- Use double buffering to hide DDR latencies.
- Use coarse-grain software pipelining to hide computations.



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# SYSTEMS OF UNIFORM RECURRENCE EQUATIONS

# SURE: system of uniform recurrence equations (1967)

Karp, Miller, Winograd: "The organization of computations for uniform recurrence equations" (J. ACM, 14(3), pp. 563-590).

$$\forall \vec{p} \in \{ \vec{p} = (i,j) \mid 1 \le i,j \le N \}$$

$$\begin{cases} a(i,j) = c(i,j-1) \\ b(i,j) = a(i-1,j) + b(i,j+1) \\ c(i,j) = a(i,j) + b(i,j) \end{cases}$$



- RDG (reduced dependence graph)  $G = (V, E, \vec{w})$ .
- EDG (expanded dep. graph): vertices  $V \times P$  = unrolled RDG.

Semantics:

- Explicit dependences, implicit schedule.
- Compute left-hand side first, unless not in  $\mathcal{P}$  (input data).

## Two main problems: computability & scheduling

Computability (KMW view) A SURE is computable for all bounded domains P if and only if the RDG has no cycle C with  $\vec{w}(C) = \vec{0}$ . Scheduling (dual view): Lamport, Feautrier, etc. How to find an explicit schedule? With guaranteed "latency"?

Looking for an elementary cycle of zero weight: NP-complete. Looking for a multi-cycle of zero weight: polynomial. Looking for a cycle of zero weight: polynomial.

## Two main problems: computability & scheduling

Computability (KMW view) A SURE is computable for all bounded domains P if and only if the RDG has no cycle C with  $\vec{w}(C) = \vec{0}$ . Scheduling (dual view): Lamport, Feautrier, etc. How to find an explicit schedule? With guaranteed "latency"?

Looking for an elementary cycle of zero weight: NP-complete. Looking for a multi-cycle of zero weight: polynomial. Looking for a cycle of zero weight: polynomial.

Key structure: the subgraph G' induced by all edges that belong to a multi-cycle (i.e., union of cycles) of zero weight.



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## Key properties for multi-dimensional decomposition

## Lemma (Look in G')

A zero-weight cycle is a zero-weight multi-cycle. ► Look in the subgraph G' only.

Note: clear, but how to compute G'?

#### Lemma (Look in each SCC)

A zero-weight cycle belongs to a strongly connected component.

Look in each strongly connected component (SCC) separately.

Note: this is the recursive step.

#### Lemma (End of recursion)

If G' is strongly connected, there is a zero-weight cycle.

This stops the recursion.

## Key properties for multi-dimensional decomposition

### Lemma (End of recursion)

If G' is strongly connected, there is a zero-weight cycle.



- ∑<sub>i</sub> e<sub>i</sub> cycle that visits all vertices.
- $e_i$  in multi-cycle  $C_i$ , with  $\vec{w}(C_i) = \vec{0}$ .
- $C_i = e_i + P_i + C'_i$ .
- Follow the  $e_i$ , then the  $P_i$  and, on the way, plug the  $C'_i$ .

## Karp, Miller, and Winograd's decomposition

Boolean KMW(G):

- Build G' the subgraph of zero-weight multicycles of G.
- Compute  $G'_1, \ldots, G'_s$ , the s SCCs of G'.
  - If s = 0, G' is empty, return TRUE.
  - If s = 1, G' is strongly connected, return FALSE.
  - Otherwise return  $\wedge_i KMW(G'_i)$  (logical AND).

Then, G is computable iff KMW(G) returns TRUE.

## Karp, Miller, and Winograd's decomposition

Boolean KMW(G):

- Build G' the subgraph of zero-weight multicycles of G.
- Compute  $G'_1, \ldots, G'_s$ , the s SCCs of G'.
  - If s = 0, G' is empty, return TRUE.
  - If s = 1, G' is strongly connected, return FALSE.
  - Otherwise return  $\wedge_i KMW(G'_i)$  (logical AND).

Then, G is computable iff KMW(G) returns TRUE.

Depth d = 0 if G acyclic, d = 1 if all SCCs have an empty G', etc.

### Theorem (Depth of the decomposition)

If G is computable,  $d \leq n$  (dimension of  $\mathcal{P}$ ). Otherwise,  $d \leq n+1$ .

## Theorem (Optimal number of parallel loops)

If  $\Omega(N) \Box \subseteq \mathcal{P} \subseteq O(N) \Box$ , there is a dependence path of length  $\Omega(N^d)$  and one can build an affine schedule of latency  $O(N^d) \bullet$  "optimal"

## But how to compute G'? Primal and dual programs.

 $e \in G'$  iff  $v_e = 0$  in any optimal solution of the linear program:

$$\mathsf{min}\left\{ \begin{array}{l} \sum_e \mathsf{v}_e \mid \vec{q} \geq \vec{0}, \ \vec{v} \geq \vec{0}, \ \vec{q} + \vec{v} \geq \vec{1}, \ C\vec{q} = \vec{0}, \ W\vec{q} = \vec{0} \end{array} \right\}$$

Always interesting to take a look at the dual program:

$$\max\left\{ \sum_{e} z_{e} \mid \vec{0} \leq \vec{z} \leq \vec{1}, \ \vec{X}.\vec{w}(e) + \rho_{v} - \rho_{u} \geq z_{e}, \ \forall e = (u, v) \in E \right\}$$

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Always interesting to take a look at the dual program:

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• Generalizes modulo scheduling:  $\sigma(u, \vec{p}) = \vec{X} \cdot \vec{p} + \rho_u$  (in 1D:  $\lambda \cdot p + \rho_u$ ). For any optimal solution:

• 
$$e \notin G' \Leftrightarrow \vec{X}.\vec{w}(e) + \rho_v - \rho_u \ge 1$$
   
•  $e \in G' \Leftrightarrow \vec{X}.\vec{w}(e) + \rho_v - \rho_u = 0$    
• loop carried.  
• loop independent.

and keep going until all dependences become carried.

Multi-dimensional scheduling and loop transformations.

## Scheduling/parallelization of illustrating example



$$\begin{cases} \vec{X}_{1.}(0,1) = 0\\ \vec{X}_{1.}(1,0) \ge 2 \end{cases} \Rightarrow \begin{cases} \vec{X}_{1} = (2,0), \ \rho_{a} = 1\\ \rho_{b} = 0, \ \rho_{c} = 1 \end{cases}$$
Final schedule 
$$\begin{cases} \sigma_{a}(i,j) = (2i+1,2j)\\ \sigma_{b}(i,j) = (2i,-j)\\ \sigma_{c}(i,j) = (2i+1,2j+1) \end{cases}$$

$$\forall \vec{p} \in \{\vec{p} = (i,j) \mid 1 \leq i,j \leq N\}$$

$$\begin{cases} a(i,j) = c(i,j-1) \\ b(i,j) = a(i-1,j) + b(i,j+1) \\ c(i,j) = a(i,j) + b(i,j) \end{cases}$$

DO i=1, N  
DO j=N, 1, -1  

$$b(i,j) = a(i-1,j) + b(i,j+1)$$
  
ENDDO  
DO j=1, N  
 $a(i,j) = c(i,j-1)$   
 $c(i,j) = a(i,j) + b(i,j)$   
ENDDO  
ENDDO

## Scheduling/parallelization of illustrating example



$$\begin{split} \vec{X_{1}}.(0,1) &= 0\\ \vec{X_{1}}.(1,0) &\geq 2 \end{split} \right\} \Rightarrow \begin{cases} \vec{X_{1}} &= (2,0), \ \rho_{a} &= 1\\ \rho_{b} &= 0, \ \rho_{c} &= 1 \end{cases} \\ \\ \hline \text{Final schedule} \begin{cases} \sigma_{a}(i,j) &= (2i+1,2j)\\ \sigma_{b}(i,j) &= (2i,-j)\\ \sigma_{c}(i,j) &= (2i+1,2j+1) \end{cases} \end{cases}$$

$$\forall \vec{p} \in \{ \vec{p} = (i,j) \mid 1 \le i,j \le N \}$$

$$\begin{cases} a(i,j) = c(i,j-1) \\ b(i,j) = a(i-1,j) + b(i,j+1) \\ c(i,j) = a(i,j) + b(i,j) \end{cases}$$

DO i=1, N  
DO j=N, 1, -1  

$$b(i,j) = a(i-1,j) + b(i,j+1)$$
  
ENDDO  
DO j=1, N  
 $a(i,j) = c(i,j-1)$   
 $c(i,j) = a(i,j) + b(i,j)$   
ENDDO  
ENDDO

 Today: most work based on Farkas lemma (affine form) following Feautrier (1992) & generalized tiling as Pluto (2008).

# DETECTION OF LOOP PARALLELISM

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## Back to DO loops: dependence distances

#### Fortran DO loops:

- Explicit schedule
- Implicit dependences
- EDG:  $S(\vec{i}) \Rightarrow T(\vec{j})$ .
- RDG:  $S \rightarrow T$ .

DO i=1, N DO j=1, N a(i,j) = ... b(i,j) = a(j,i) + 1 ENDDO ENDDO Pair set  $R_{S,T} = \{(\vec{i},\vec{j}) \mid S(\vec{i}) \Rightarrow T(\vec{j})\}$ Affine dep.  $\vec{i} = f(\vec{j})$  when possible. Distances  $E_{S,T} = \{(\vec{j} - \vec{i}) \mid S(\vec{i}) \Rightarrow T(\vec{j})\}.$ 

## Over-approx. $\overline{E}_{S,T}$ s.t. $E_{S,T} \subseteq \overline{E}_{S,T}$ :

- affine relation
- polyhedron: vertices, rays, lines
- direction vector:  $\mathbb{Z}$ , +, -, \*
- dependence level: 1, 2, …,  $\infty$

## Back to DO loops: dependence distances

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Polyhedral approximation: 
$$E' = \left\{ \begin{pmatrix} 1 \\ -1 \end{pmatrix} + \lambda \begin{pmatrix} 1 \\ -1 \end{pmatrix} \middle| \lambda \ge 0 \right\}$$
  
Direction vector:  $E' = \begin{pmatrix} + \\ - \end{pmatrix} = \left\{ \begin{pmatrix} 1 \\ -1 \end{pmatrix} + \lambda \begin{pmatrix} 1 \\ 0 \end{pmatrix} + \mu \begin{pmatrix} 0 \\ -1 \end{pmatrix} \middle| \lambda, \mu \ge 0 \right\}$   
Level:  $E' = \bigcirc = \begin{pmatrix} + \\ * \end{pmatrix} = \left\{ \begin{pmatrix} 1 \\ 0 \end{pmatrix} + \lambda \begin{pmatrix} 1 \\ 0 \end{pmatrix} + \mu \begin{pmatrix} 0 \\ 1 \end{pmatrix} \middle| \lambda \ge 0 \right\}$   
 $53/98$ 

## Uniformization of dependences: example

```
DO i=1, N

DO j=1, N

S: a(i,j) = c(i,j-1)

T: c(i,j) = a(i,j) + a(i-1,N)

ENDDO

ENDDO
```

 $S(i-1,N) \Rightarrow T(i,j)$ Dep. distance (1, j - N).

## Uniformization of dependences: example



No parallelism (d = 2). Code appears purely sequential (and here it is).

## Second example with direction vectors

DO i= 1, N  
DO j = 1, N  
DO k = 1, j  
S1: 
$$a(i,j,k) = c(i,j,k-1) + 1$$
  
S2:  $b(i,j,k) = a(i-1,j+i,k) + b(i,j-1,k)$   
S3:  $c(i,j,k+1) = c(i,j,k) + b(i,j-1,k+i) + a(i,j-k,k+1)$   
ENDDO  
ENDDO  
ENDDO  
ENDDO  
ENDDO

## Second example: dependence graphs



Initial RDG.



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## Second example: G and G'



## Second exemple: parallel code generation

```
DOSEQ i=1, n
  DOSEQ j=1, n /* scheduling (2i, j) for S2^*/
    DOPAR k=1, j
      S2: b(i,j,k) = a(i-1,j+i,k) + b(i,j-1,k)
    FNDDOPAR
  ENDDOSEQ
  DOSEQ k = 1, n+1
    IF (k \leq n) THEN /* scheduling (2i+1, 2k) for S1*/
      DOPAR j=k, n
        S1: a(i,j,k) = c(i,j,k-1) + 1
      ENDDOPAR
    IF (k > 2) THEN /* scheduling (2i+1, 2k+3) for S3*/
      DOPAR j=k-1, n
        S3: c(i,j,k) = c(i,j,k-1) + b(i,j-1,k+i-1) + a(i,j-k+1,k)
      FNDDOPAR
  ENDDOSEQ
ENDDOSEQ
                   > Loop distribution of j, k loops: S_2 then S_1 + S_3.
                   > Loop interchange of j and k loops for S_1 and S_3.
                   > Loop shifting in k, then loop distribution of j loop.
```

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# Allen-(Callahan)-Kennedy (1987): loop distribution

AK(G, k):

- Remove from G all edges of level < k.
- Compute  $G_1, \ldots, G_s$  the s SCCs of G in topological order.
  - If  $G_i$  has a single statement S, with no edge, generate DOPAR loops in all remaining dimensions, and generate code for S.
  - Otherwise:
    - Generate DOPAR loops from level k to level l 1, and a DOSEQ loop for level l, where l is the minimal level in  $G_i$ .
    - call AK(G<sub>i</sub>, I+1). /\* d<sub>5</sub> sequential loops for statement S \*/

▶ Variant of (dual of) KMW with DOPAR as high as possible.

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    - call AK(G<sub>i</sub>, l + 1). /\*  $d_S$  sequential loops for statement S \*/
- > Variant of (dual of) KMW with DOPAR as high as possible.

### Theorem (Optimality for AK w.r.t. dependence levels)

Nested loops  $\mathcal{L}$ , RDG G with levels. One can build some nested loops  $\mathcal{L}'$ , with same structure as  $\mathcal{L}$  and same RDG as G, with bounds parameterized by N such that, for each SCC G<sub>i</sub> of G, there is a path in the EDG of  $\mathcal{L}'$  that visits  $\Omega(N^{d_s})$  times each statement S of G<sub>i</sub> (d<sub>S</sub>: depth w.r.t. S).

## Darte-Vivien (1997): unimodular + shift + distribution

Boolean DV(G, k) /\* G uniformized graph, with virtual and actual nodes \*/

- Build G' generated by the zero-weight multi-cycles of G.
- Modify slightly G' (technical detail not explained here).
- Choose  $\vec{X}$  (vector) and, for each S in G',  $\rho_S$  (scalar) s.t.:

 $\left\{ \begin{array}{l} \text{if } e = (u, v) \in G' \text{ or } u \text{ is virtual}, \ \vec{X}. \vec{w}(e) + \rho_v - \rho_u \geq 0 \\ \text{if } e \notin G' \text{ and } u \text{ is actual}, \ \vec{X}. \vec{w}(e) + \rho_v - \rho_u \geq 1 \end{array} \right.$ 

For each actual node S of G let  $\rho_S^k = \rho_S$  and  $\vec{X}_S^k = \vec{X}$ .

- Compute  $G_1'$ , ...,  $G_s'$  the SCC of G' with  $\geq 1$  actual node:
  - If G' is empty or has only virtual nodes, return TRUE.
  - If G' is strongly connected with  $\geq 1$  actual node, return FALSE.
  - Otherwise, return  $\bigwedge_{i=1} DV(G'_i, k+1)$  ( $\bigwedge = \text{logical AND}$ ).

**\blacktriangleright** Dual of KMW after dependence uniformization. Analyzing the cycle weights in G' leads to a variant to get a max. number of permutable loops.

## General affine multi-dimensional schedules (Feautrier)

Affine dependences (or even relations):  $T(\vec{j})$  depends on  $S(\vec{i})$  if  $(\vec{i}, \vec{j}) \in D_e$ where e = (S, T) and  $D_e$  is a polyhedron.

- Look for affine schedule  $\sigma$  such that  $\sigma(S, \vec{i}) <_{lex} \sigma(T, \vec{j})$  for all  $(\vec{i}, \vec{j}) \in \mathcal{D}_e$ . Use affine form of Farkas lemma (mechanical operation).
- Write  $\sigma(S, \vec{i}) + \epsilon_e \leq \sigma(T, \vec{j})$  with  $\vec{\epsilon} \geq \vec{0}$  and maximize the number of dependence edges e such that  $\epsilon_e \geq 1$ .
- Remove edges e such that e<sub>e</sub> ≥ 1 and continue to get remaining dimensions 

   multi-dimensional affine schedule.
- Generalization of the constraints used in the dual of KMW.

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   multi-dimensional affine schedule.

#### ➡ Generalization of the constraints used in the dual of KMW.

To perform tiling, look for several dimensions (permutable loops) such that  $\sigma(T, \vec{j}) - \sigma(S, \vec{i}) \ge 0$  instead of  $\sigma(T, \vec{j}) - \sigma(S, \vec{i}) \ge 1$ . But more complicated to avoid the  $\vec{0}$  solution and guarantee linear independence. Key idea in Pluto: minimize dependence distance  $\sigma(T, \vec{j}) - \sigma(S, \vec{i})$ .

- Lamport (1974) hyperplane scheduling = skewing, interchange.
- Allen-Kennedy (1987) loop distribution, optimal for levels.
- Wolf-Lam (1991) unimodular, optimal for direction vectors and one statement. Based on finding permutable loops.
- Feautrier (1992) general affine scheduling, complete for affine dependences and affine transformations, but not optimal. Relies on Farkas lemma.
- Darte-Vivien (1997) unimodular, shift, distribution, optimal for polyhedral abstraction of distances. Finds permutable loops, too.
- Lim-Lam (1998) extension to coarse-grain parallelism, vague.
- Bondhugula-Ramanujam-Sadayappan (2008) improved extension, permutable loops (tiling), locality optimization. 
  Pluto compiler. Principle: look for maximum number of linearly-independent solutions with nonnegative dependence distance. Tile bands.

#### Fortran DO loops:

#### Uniform recurrence equations:

$$\forall p \in \{ p = (i,j) \mid 1 \le i,j \le N \}$$

$$\begin{cases} a(i,j) = c(i,j-1) \\ b(i,j) = a(i-1,j) + b(i,j+1) \\ c(i,j) = a(i,j) + b(i,j) \end{cases}$$

#### C for and while loops:

# KERNEL OFFLOADING AND LOOP TILING

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Industrial tools: pretty good for optimizing computation kernel But still a huge problem for feeding the accelerators with data.

Our idea ( $\sim$ 2009): use HLS tools as back-end compilers, assuming it puts the necessary computing resources to be limited by bandwidth.

- Push all the dirty work in the back-end compiler.
- Optimize transfers at C level.
- Compile any new functions with the same HLS tool.

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Use Altera C2H as a back-end compiler. Main features:

- Syntax-directed translation to hardware:
  - Local array = local memory, other arrays/pointers = external memory.
  - Hierarchical FSMs: outer FSM stalls to wait for the latest inner FSM.
- Software pipelined loops:
  - Basic software pipelining with rough data dependence analysis.
  - Latency-aware pipelined DDR accesses (with internal FIFOs).
- Full interface within the complete system:
  - Accelerator(s) initiated as (blocking or not) function call(s).
  - Possibility to define FIFOs between accelerators.

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Similar study Pouchet et al. FPGA'13 for Xilinx AutoESL

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# Throughput when accessing (asymmetric) DDR memory

Ex: DDR-400 128Mbx8, size 16MB, CAS 3, 200MHz. Successive reads, same row = 10 ns, different rows = 80 ns. Even if fully pipelined ( $\lambda$ =1), a bad spatial DDR locality can kill performances by a factor 8! Example:

```
void vector_sum (int* __restrict__ a, b, c, int n) {
   for (int i = 0; i < n; i++) c[i] = a[i] + b[i];</pre>
```





C2H-compiled code: pipelined but time gaps & data thrown away.

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Block version: reduces gaps, exploits bursts and temporal reuse.

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}</pre>
```

```
PRECHARGE
                                   block size
                                                PRECHARGE
                         READ
               ACTIVATE
                                                                                                 ACTIVATE
/RAS
/CAS
/WF
                                          a(i+k)
                                                                                    lb(i+k
                                                                                                                              lc(i+k
DO
                                                                load b(i) ... b(i+k)
                      load a(i) ... a(i+k)
                                                                                                       store c(i) ... c(i+k)
```

Block version: reduces gaps, exploits bursts and temporal reuse.



Typical figure with speed-up vs block size (here vector sum).

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# Strip-mining and loop distribution?

Loop distribution: too large local memory. Larolling: too many registers.



```
for (i=0; i<MAX; i=i+BLOCK) {</pre>
  for(j=0; j<BLOCK; j++) a_tmp[j] = a[i+j]; //prefetch</pre>
  for(j=0; j<BLOCK; j++) b_tmp[j] = b[i+j]; //prefetch</pre>
  for(j=0; j<BLOCK; j++) c_tmp[i+j] = a_tmp[j] + b_tmp[j];</pre>
  for(j=0; j<BLOCK; j++) c[i+j] = c_tmp[i+j]; //store</pre>
}
```

# Strip-mining and loop distribution?

Loop distribution: too large local memory. Unrolling: too many registers. strip-mining + loop distribution.

```
for (i=0; i<MAX; i=i+BLOCK) {
   for(j=0; j<BLOCK; j++) a_tmp[j] = a[i+j]; //prefetch
   for(j=0; j<BLOCK; j++) b_tmp[j] = b[i+j]; //prefetch
   for(j=0; j<BLOCK; j++) c_tmp[i+j] = a_tmp[j] + b_tmp[j];
   for(j=0; j<BLOCK; j++) c[i+j] = c_tmp[i+j]; //store
}</pre>
```



#### Does not work!

- Accesses to arrays a and b still interleaved!
- Loop latency penalty.
- Outer loop not pipelined.



Still pay loop latency penalty and poor outermost loop pipeline.

# Emulating (linearizing) nested loops?

```
i=0; j=0; bi=0;
for (k=0; k<4*MAX; k++) {
    if (j==0) a_tmp[i] = a[bi+i];
    else if (j==1)
        b_tmp[i] = b[bi+i];
    else if (j==2)
        c_tmp[i] = a_tmp[i] + b_tmp[i];
    else c[bi+i] = c_tmp[i];
    if (i<BLOCK-1) i++;</pre>
```

```
else {
    i=0;
    if (j<3) j++;
    else {j=0; bi = bi + BLOCK;}
}</pre>
```

}

- Need to use *restrict* pragma for all arrays.
- $\lambda = 21!$  Problem with dependence analyzer and software pipeliner.
- Better behavior (λ = 3) with case statement: by luck.
- Further loop unrolling to get  $\lambda = 1$ : too complex.
- But still a problem with interleaved DDR accesses due to speculative prefetching!

## Emulating nested loops with a single transfer instruction?

- No more interleaving between arrays a and b;
- λ not equal to 1, unless *restrict* pragma added: but leads to potentially wrong codes (data dependences are lost).

How to decrease  $\lambda$  and generalize to more complex codes?

Communicating C processes, with suitable synchronizations.

How to optimize transfers automatically?



How to optimize transfers automatically? With C-level processes.



How to optimize transfers automatically? With C-level processes.



General problem: porting applications on hardware accelerators

- Ex: FPGA, GPU, dedicated board, multicore.
- Huge portability issue, costly compiler development.

How to optimize transfers automatically? With C-level processes.



General problem: porting applications on hardware accelerators

- Ex: FPGA, GPU, dedicated board, multicore.
- Huge portability issue, costly compiler development.

Kernel offloading/function outlining

- High-productivity and high-performance languages.
- Library/directives-type support, e.g., OpenAcc.
- Source-to-source compilation, targeting back-end C dialects.

# Data Movement between Memory Levels



- CPU Multi-level cache optimization
- GPU Host to Global / Global to Shared / Shared to registers
- MPPA External DDR to multi scratch-pads
- FPGA External DDR to local memory



- CPU Multi-level cache optimization
- GPU Host to Global / Global to Shared / Shared to registers
- MPPA External DDR to multi scratch-pads
- FPGA External DDR to local memory
  - Computation by blocks 
     loop tiling
  - Transfer optimization 🖝 intra-tile & inter-tile data reuse

  - Cost model 🖝 parametric tile sizes

## Tiling, Data Reuse, and Pipelining



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## Tiling, Data Reuse, and Pipelining



## Tiling, Data Reuse, and Pipelining



# Kernel offloading with parametric tiling & double buffering



```
int i,j;
for(i = 0; i < n; i++) {
  for(j = 0; j < n; j++) {
    C[i+j] = C[i+j] + A[i]*B[j];
  }
}
```

- Pipelining of tiles.
- Computation of loads/stores.
- Intra- and inter-tile data reuse.

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- Pipelining of tiles.
- Computation of loads/stores.
- Intra- and inter-tile data reuse.

 Parametric (not quadratic, but piece-wise affine), with possible approximations, corresponding liveness analysis, and memory mapping.



Product of two polynomials:

- arguments in A and B;
- result in C.
- dep. distance (1, -1). prevents permutation.

```
for (i=0, i<=2n-1; i++)
c[i] = 0;
for (i=0; i<n; i++)
for (j=0; j<n; j++)
c[i+j] = c[i+j] + A[i]*B[j];</pre>
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```
Order: lexico along (i + j, j).
```



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Order: lexico along (n - j - 1, i).



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• arguments in A and B;

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 mow (1, 1), (1, 0), (0, 1).

Order: lexico along (n - j - 1, i). Tiling:  $(\lfloor \frac{n-j-1}{s_1} \rfloor, \lfloor \frac{i}{s_2} \rfloor, n - j - 1, i)$ .



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Initial paper: "Supernote partitioning", F. Irigoin, R. Triolet, ICS'88. Permutability condition:

• Dependences not loop-carried are not relevant. Indeed,  $(\vec{0}, \vec{d})$  remains unchanged, thus lexicopositive.

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Tiling validity: After tiling,  $\vec{i} \mapsto (\vec{l}, \vec{ii}) = (\lfloor \vec{i}/\vec{s} \rfloor, \vec{i} \mod \vec{s})$ . Furthermore:

$$ec{j} \geq ec{i} \Rightarrow ec{j} - ec{i} \geq ec{0} \Rightarrow (ec{j} - ec{i})/ec{s} \geq ec{0} \Rightarrow ec{j}/ec{s} \geq ec{i}/ec{s} \Rightarrow |ec{j}/ec{s}| \geq |ec{i}/ec{s}|$$

• Dep.  $\vec{d} \succ \vec{0}$  becomes  $\vec{d}' \succeq \vec{0}$ . Tiles can still be scheduled.



Valid: yes

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#### "Ratio" of computation and communication volume

"Pen-ultimate Tiling?", P. Boulet, A. Darte, T. Risset, Y. Robert, Integration J., 1994.

Tile shape given by tile edges. Ex: 
$$P = \begin{pmatrix} 2 & 1 \\ 0 & 3 \end{pmatrix}$$
.  $H = P^{-1}$   
 $H = \frac{1}{6} \begin{pmatrix} 3 & -1 \\ 0 & 2 \end{pmatrix}$ . With  $D = \begin{pmatrix} 1 & 1 \\ 0 & 1 \end{pmatrix}$ ,  $HD = \frac{1}{6} \begin{pmatrix} 3 & 2 \\ 0 & 2 \end{pmatrix} \ge \vec{0}$ .

Tile computation volume equal to  $|\det P| = 1/|\det H|$ .

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Tile communication volume roughly  $\frac{\sum_{i=1}^{n} \sum_{j=1}^{m} (HD)_{i,j}}{|\det H|}$ . Indeed:  $|\det(d, p_2, \dots, p_n)| = |(p_2 \wedge \dots \wedge p_n).d| = |(\det P)h_1.d| = |\det P|(h_1.d)$ 

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Aspect ratio Minimize communication for a given computation volume.  
Minimize  $\frac{\sum_{i=1}^{n} \sum_{j=1}^{m} (HD)_{i,j}}{|\det H|^{\frac{1}{n}}}$  subject to  $\det H \neq 0$ ,  $HD \ge \vec{0}$ .
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Aspect ratio Minimize communication for a given computation volume.

Minimize  $\frac{\sum_{i=1}^{n} \sum_{j=1}^{n} (HD)_{i,j}}{|\det H|^{\frac{1}{n}}}$  subject to det  $H \neq 0$ ,  $HD \ge \vec{0}$ . Solvable!

• If D is square, non singular, opt. for  $H = D^{-1}$  and ratio  $n |\det D|^{\frac{1}{n}}$ .

• General case: cone C(D), opt. for *n* generators of  $C^*(D)$ , scaled to induce the same communication on all faces.

#### Generating loop bounds for tiled codes

- "Scanning Polyhedra with DO Loops", Ancourt, Irigoin, PPoPP'91.
- "An Efficient Code Generation Technique for Tiled Iteration Spaces", Goumas, Athanasaki, Koziris, IEEE TPDS, 2003.
- "Parameterized Tiled Loops for Free", Renga., Kim, Rajopadhye, Strout, PLDI'07.

Tile of size  $\vec{s}$  with origin  $\vec{i_0}$ :  $\{\vec{i} \mid \vec{i_0} \leq \vec{i} \leq \vec{i_0} + \vec{s} - \vec{1}\}$ .

Elementary bounding box method: many empty tiles.

```
//Original code //Skewed code
for(t=1; t<=M; t++) for(i=2; i<=N; i++) for(k=2+t; k<=N+t; k++)
    S(t,i); S(t,k-t);</pre>
```

```
//Tiled code, many empty iterations
for(T=1; T<=M; T+=st)
  for(K=3; K<=N+M; K+=sk}
   for(t=max(T,1); t<=min(T+st-1,M); t++)
      for(k=max(K,2+t); k<=min(K+sk-1,N+t); k++)
            S(t,k-t);</pre>
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Exact computation of non-empty tiles for fixed tile sizes.

//Skewed code
<pre>for(t=1; t&lt;=M; t++)</pre>
<pre>for(k=2+t; k&lt;=N+t; k++)</pre>
S(t,k-t);

Code not depicted. Only for fixed tile sizes. Express the lattice  $\mathcal{L}(\vec{s})$  of all tile origins  $\vec{i}_0 = \vec{0} \mod \vec{s}$ , and project existential variables.

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```
Approx. iterations \{\vec{z} \mid Q\vec{z} \geq \vec{b}\} by the "outer set" \{\vec{z} \mid Q\vec{z} + Q^+\vec{s} \geq \vec{b}\}.
//Skewed code
                                                        Outer set shift:
for(t=1; t<=M; t++)</pre>
                                           • 1 < t < M \Rightarrow 2 - st < t < M
  for(k=2+t: k<=N+t: k++)</pre>
    S(t,k-t):
                                           • 2 < k-t < N \Rightarrow 3-sk < k-t < N+st-1
//Tiled code, fewer empty iterations
LBT = 2-st; LBT = ceil(LBT/st)*st;
for(T=LBT; T<=M; T+=st) {</pre>
  LBK = 3+t-sk; LBK = ceil(LBK/sk)*sk;
  for(K=LBK; K<=N+t+st-1; K+=sk}</pre>
    for(t=max(T,1); t<=min(T+st-1,M); t++)</pre>
      for(k=max(K,2+t); k<=min(K+sk-1,N+t); k++)</pre>
         S(t,k-t):
                                                           イロト 不得 トイヨト イヨト ヨー うらつ
}
```

# INTER-TILE DATA REUSE AND LOCAL STORAGE

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#### Definition

- Load(T): data loaded from DDR just before executing tile T.
- Store(T): data stored to DDR just after T.
- In(T): input data for T, i.e., read before being possibly written in T.
- Out(T): output data for T, i.e., data written in T.

#### Minimal dependence structure



#### Goals

- Reuse local data: intra- and inter-tile reuse in a tile strip.
- Do not store back after each write: external memory not up-to-date.
- Minimize live-ranges in local memory: need local memory allocation.







# Inter-tile data reuse enables pipelining









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Computations can be done with iscc.

#### Some operations may execute

- if conditions that are not analyzable.
- Some data may be accessed
  - access functions that are not fully analyzable.

Approximated  $\ln/Out$  sets for tiles  $\bullet$   $\overline{In}$ ,  $\overline{Out}$ ,  $\underline{Out}$ .

- due to the analysis (e.g., array regions);
- by choice to represent simpler sets (e.g., hyper-rectangles);
- to simplify the analysis (e.g., Fourier-Motzkin).

Approximated Load/Store sets restriction Formatter Formatter Store, Load.

- to simplify code generation;
- to perform communications by blocks;
- to simplify memory allocation;

• . . .

Problem:

- Tile T may write X, i.e.,  $X \in \overline{\text{Out}}(T)$
- Tile T' may read X, i.e.,  $X \in \overline{\mathrm{In}}(T')$
- $\bullet$  Only T and T' may access X

Should we load X? When?

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- Only T and T' may access X

Should we load X? When?

- T' happens before T 
   Ioad before T'
- T' happens after T and  $X \in \underline{Out}(T)$   $\checkmark$  do not load
- T' happens after T and  $X \notin \underline{Out}(T) =$  load before T





F defined at tile level.

Can we use the same trick as for the exact case?

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 $\mathcal{C} \text{ set of all tiles, } \mathcal{C}_1, \mathcal{C}_2 \subseteq \mathcal{C} \\ \text{such that } \bigcup_{T \in \mathcal{C}_1} T = \bigcup_{T \in \mathcal{C}_2} T$ 

$$\bigcup_{T\in\mathcal{C}_1}F(T)\stackrel{?}{=}\bigcup_{T\in\mathcal{C}_2}F(T)$$

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$$\bigcup_{T\in\mathcal{C}_1}F(T)\stackrel{?}{=}\bigcup_{T\in\mathcal{C}_2}F(T)$$

Iff *F* is point-wise:

$$\exists f, \forall T \in \mathcal{C}, F(T) = \bigcup_{x \in T} f(x)$$

similar to the exact case.

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</p>

# Simple script with iscc

```
# Inputs
Params := [M, N, s_1, s_2] \rightarrow \{ : s_1 \ge 0 \text{ and } s_2 \ge 0 \};
Domain := [M, N] -> { # Iteration domains
  S_1[i_1, i_2] : 1 <= i_2 <= N-2 and 0 <= i_1 <= M-1;
  S_2[i_1, i_2] : 1 <= i_2 <= N-2 and 0 <= i_1 <= M-1;
} * Params:
Read := [M, N] -> { # Read access functions
  S_1[i_1, i_2] \rightarrow A[m] : -1 + i_2 \le m \le 1 + i_2;
                                                                 # Set/relation computations
  S_2[i_1, i_2] -> B[i_2]; } * Domain;
                                                                TiledRead := Tiling.(Theta^-1).Read;
                                                                TiledWrite := Tiling.(Theta^-1).Write;
Write := [M, N] -> { # Write access functions
  S_1[i_1, i_2] \rightarrow B[i_2];
                                                                In := Coalesce.(TiledRead - (Prev.TiledWrite));
  S_2[i_1, i_2] -> A[i_2]; } * Domain;
                                                                Out := Coalesce.TiledWrite:
Theta := [M, N] -> { # Preliminary mapping
                                                                Load := In - ((TiledPrev.In) + (TiledPrev.Out));
  S_1[i_1, i_2] \rightarrow [i_1, 2 i_1 + i_2, 0];
                                                                 Store := Out - (TiledNext.Out):
  S_2[i_1, i_2] \rightarrow [i_1, 1 + 2 i_1 + i_2, 1]; 
                                                                 print coalesce (Load % Params):
                                                                 print coalesce (Store % Params);
# Tools for set manipulations
Tiling := [s_1, s_2] \rightarrow \{ \# \text{ Two dimensional tiling} \}
  [[I 1, I 2] -> [i 1, i 2, k]] -> [i 1, i 2, k] :
      I 1 \le i 1 \le I 1 + s 1 and I 2 \le i 2 \le I 2 + s 2;
Coalesce := { [I_1, I_2] -> [[I_1, I_2] -> [i_1, i_2, k]] };
Strip := { [I_1, I_2] -> [I_1, I_2'] };
Prev := { # Lexicographic order
  [[I_1, I_2] \rightarrow [i_1, i_2, k]] \rightarrow [[I_1, I_2] \rightarrow [i_1', i_2', k']]
      i_1' \le i_1 - 1 or (i_1' \le i_1 \text{ and } i_2' \le i_2 - 1)
      or (i 1' <= i 1 and i 2' <= i 2 and k' <= k - 1) };
TiledPrev := [s_1, s_2] -> { # Special ''lexicographic'' order
  [I_1, I_2] -> [I_1', I_2'] : I_1' <= I_1 - s_1 or
      (I 1' <= I 1 and I 2' <= I 2 - s 2) } * Strip:
TiledNext := TiledPrev^-1:
```

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$$\begin{aligned} \text{Load}(\vec{l}) &= \{ A(m) \mid 1 \le m + 2l_1 - l_2 \le s_2, \, s_1 \ge 1, \, l_1 \ge 0, \, m \ge 1, \, l_1 \le -1 + M, \\ l_2 \ge 2 - s_2 + 2l_1, \, m \le -1 + N, \, N \ge 3 \} \\ &\cup \{ A(m) \mid m \ge 1 + l_2, \, m \ge 1, \, M \ge 1, \, m \le -1 + N, \, l_1 \le -1, \\ l_1 \ge 1 - s_1, \, l_2 \ge 2 - s_2, \, N \ge 3, \, m \le s_2 + l_2 \} \\ &\cup \{ A(1) \mid l_2 = 1 + 2l_1 \land 0 \le l_1 \le -1 + M, \, N \ge 3, \, s_1 \ge 1, \, s_2 \ge 1 \} \\ &\cup \{ A(m) \mid 0 \le m \le 1, \, l_2 = 1 \le s_2, \, 1 - s_1 \le l_1 \le -1, \, M \ge 1, \, N \ge 3 \} \\ &\cup \{ A(0) \mid 0 \le l_1 \le M - 1, \, N \ge 3, \, s_1 \ge 1, \, 1 \le l_2 - 2l_1 \ge 2 - s_2 \} \\ &\cup \{ A(0) \mid 1 - s_1 \le l_1 \le -1, \, M \ge 1, \, N \ge 3, \, l_2 \ge 2 - s_2, \, l_2 \le 0 \} \end{aligned}$$

Store(1) = {B(m) | 
$$m \ge 1, m \ge 2 - 2M + s_2 + l_2, m \le -2 + N,$$
  
 $l_1 \ge 1 - s_1, 2 \le m + 2s_1 + 2l_1 - l_2 \le 1 + s_2, s_1 \ge 1$ }  
 $\cup$  {B(m) |  $m \ge 1, s_1 \ge 1, m \le -2 + N, l_1 \le -1 + M, m \le 1 - 2M + s_2 + l_2,$   
 $m \ge 2 - 2s_1 - 2l_1 + l_2, l_1 \ge 1 - s_1, M \ge 1, m \ge 2 - 2M + l_2$ }  
 $\cup$  {A(m) |  $m \ge 1, m \ge 1 - 2M + s_2 + l_2, m \le -2 + N,$   
 $l_1 \ge 1 - s_1, 1 \le m + 2s_1 + 2l_1 - l_2 \le s_2, s_1 \ge 1$ }  
 $\cup$  {A(m) |  $m \ge 1, s_1 \ge 1, m \le -2 + N, l_1 \le -1 + M, m \le -2M + s_2 + l_2,$   
 $m \ge 1 - 2s_1 - 2l_1 + l_2, l_1 \ge 1 - s_1, M \ge 1, m \ge 1 - 2M + l_2$ }

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Sequential Memory Size	Pipelined Memory Size
jacobi-1d-imper	
$A[2s_1 + s_2]$	$A[2s_1 + 2s_2]$
$B[2s_1 + s_2 - 1]$	$B[2s_1 + 2s_2 - 2]$
jacobi-2d-imper	
$A[2s_1 + s_2, \min(2s_1, s_2 + 1) + s_3]$	$A[2s_1 + s_2, \min(2s_1, s_2 + 1) + 2s_3]$
$B[2s_1 + s_2 - 1, \min(2s_1, s_2 + 1) + s_3 - 1]$	$B[2s_1 + s_2 - 1, \min(2s_1, s_2 + 1) + 2s_3 - 2]$
seidel-2d	
$A\begin{bmatrix} s_1 + s_2 + 1, \\ min(2s_1 + 2, s_1 + s_2, 2s_2 + 2) + s_3 \end{bmatrix}$	$\mathbb{A}\begin{bmatrix} s_1 + s_2 + 1, \\ \min(2s_1 + 2, s_1 + s_2, 2s_2 + 2) + 2s_3 \end{bmatrix}$
gemm	
$\mathtt{A}[s_1, s_3]$	$A[s_1, 2s_3]$
$B[s_3, s_2]$	$B[2s_3, s_2]$
$C[s_1, s_2]$	$C[s_1, s_2]$
floyd-warshall	
$\left[ \begin{array}{c} \max(k+1,n-k),\\ \max(k+1,n-k) \end{array} \right]$	$path\left[\max(k+1, n-k), \\ \max(k+1, n-k, 2s_2)\right]$

#### Instance-wise order for sequential and parallel loops

```
for(i=0; i<n; i++) {
   for(j=0; j<n; j++) {
   S: ...
   T: ...
   }
}</pre>
```

- Total order  $\prec$  defined by a sequential schedule  $\sigma$  and lexicographic order.
- $\sigma(S(i,j)) = (i,j,0), \ \sigma(T(i,j)) = (i,j,1).$
- $O \prec O'$  iff  $\sigma(O) <_{\mathsf{lex}} \sigma(O')$ .
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for(i=0; i<n; i++) {
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# More general orders: polyhedral fragment of X10

X10 language developed at IBM, variant at Rice (V. Sarkar)

- PGAS (partitioned global address space) memory principle.
- Parallelism of threads: in particular keywords finish, async, clock.
- No deadlocks by construction but non-determinism.

```
Polyhedral X10 Yuki, Feautrier, Rajopadhye, Saraswat (PPoPP 2013) Can we analyze the code for data races?
```

```
finish {
  for(i in 0..n-1) {
    for(i in 0..n-1) {
        S1;
        async {
        S2;
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        }
    }
  }
}
```

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finish {
                                      clocked finish {
  for(i in 0..n-1) {
                                        for(i in 0..n-1) {
                                          S1; advance();
    S1:
                                          clocked async {
    async {
                                            S2; advance();
      S2;
    }
                                          }
  }
                                        }
                                      3
}
```

Yes. Similar to data-flow analysis. Partial order  $\prec$ : incomplete lexicographic order.

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}
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Yes. Similar to data-flow analysis. Partial order  $\prec$ : incomplete lexicographic order.

Undecidable. Partial order  $\prec_c$  defined by  $\vec{x} \prec_c \vec{y}$  iff  $\vec{x} \prec \vec{y}$  or  $\phi(\vec{x}) < \phi(\vec{y})$ .  $\phi(\vec{x}) = \#$  advances before (for  $\prec$ )  $\vec{x}$ .

## Liveness analysis

Uses of liveness analysis:

- Necessary for memory reuse:
  - Register allocation: interference graph.
  - Array contraction: conflicting relations.
  - Even wire usage: bitwidth analysis.
- Important information for:
  - Communication: live-in/live-out sets (inlining, offloading)
  - Memory footprint (e.g., for cache prediction)
  - Lower/upper bounds on memory usage.

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Several variants:

- Value-based or memory-based analysis.
- Liveness sets or interference graphs.
- Control flow graphs (CFG): basic blocks, SSA, SSI, etc.
- Task graphs, parallel specifications: not really explored so far.

# Array contraction: symbolic unrolling, analysis, mapping

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c + ...;

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# Array contraction: symbolic unrolling, analysis, mapping

} Mapping:  $a[i][j] \mapsto a[(j-i)\%(n+1)]$ 


## Array contraction: symbolic unrolling, analysis, mapping

for(i=0; i<n; ++i) {
 forpar(j=0; j<n; ++j) {
 A[i][j] = A[i-1][j-1] +
 A[i-1,j] + A[i-1,j+1];
 }
} Mapping: a[i][j] → a[i½][j]</pre>

c = 0; for(i=0; i<n; i++) { c = c + ...; }



#### Liveness at a given "step" with iscc

```
# Inputs
Params := [n] \rightarrow \{ : n \ge 0 \}:
Domain := [n] \rightarrow \{ S[i,j] : 0 \le i, j \le n \};
Read := [n] \rightarrow \{ S[i,j] \rightarrow A[i-1,j-1]; S[i,j] \rightarrow A[i-1,j]; \}
                     S[i,j] -> A[i-1,j+1] } * Domain;
Write := [n] \rightarrow \{ S[i,j] \rightarrow A[i,j] \} * Domain;
Sched := [n] \rightarrow \{ S[i,j] \rightarrow [i,j] \};
# Operators
Prev := { [i,j]->[k,1]: i<k or (i=k and j<1) };</pre>
Preveq := { [i,j]->[k,1]: i<k or (i=k and j<=1) };</pre>
WriteBeforeTStep := (Prev^-1).(Sched^-1).Write;
ReadAfterTStep := Preveq.(Sched^-1).Read;
# Liveness and conflicts
Live := WriteBeforeTStep * ReadAfterTStep;
Conflict := (Live<sup>-1</sup>).Live:
Delta := deltas Conflict;
     Delta(n) = \{(1, i_1) \mid i_1 < 0, n > 3, i_1 > 1 - n\} \cup
                   \{(0, i_1) \mid i_1 > 1 - n, n > 2, i_1 < -1 + n\} \cup
                   \{(-1, i_1) \mid i_1 \geq 0, n \geq 3, i_1 \leq -1 + n\}
                                                           93 / 98
```

## Generalizations? Liveness sets not the right concept

Inner parallelism Almost the same.

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Seq/Par nested loops Can use a careful hierarchical approach.

Inner parallelism Almost the same.

Seq/Par nested loops Can use a careful hierarchical approach. Software pipelining Harder to get a concept of "time".



On the right, values computed in S(i-1) and L(i+1) both conflict with those in (C, i), but not with each other. Not a clique.

## Reasoning at the level of traces

Define:

- $a \in t$  iff a is executed in a trace t;
- $a \prec_t b$  iff  $a \in t$ ,  $b \in t$  and a is executed before b in t;
- $S_{\exists}(a, b)$  iff there is a trace t such that  $a \prec_t b$ .
- $R_{\forall}(a,b) = \neg S_{\exists}(b,a)$  iff, for all traces  $t, a, b \in t$  implies  $a \prec_t b$ .

Then, a and b conflict  $(a \bowtie b)$  if, for some trace t,  $W_a \prec_t W_b \prec_t R_a$ .

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Conservative approximations for  $a \bowtie b$ :

- iff  $S_{\exists}(W_a, R_a)$ ,  $S_{\exists}(W_a, W_b)$ ,  $S_{\exists}(W_b, R_a)$  iff  $\neg R_{\forall}(R_a, W_a)$ ,  $\neg R_{\forall}(W_b, W_a)$ ,  $\neg R_{\forall}(R_a, W_b)$ .
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When 
$$\underline{R}_{\forall}$$
 is a partial order  $\preceq$ ,  $a \bowtie b$  iff  $R_a \not\prec W_a, W_b \not\prec W_a, R_a \not\prec W_b$ .

 Covers sequential code, OpenMP-like loop parallelism, OpenMP-4.0 task parallelism, X10, OpenStream, even some form of if conditions, etc.

Modulo mapping  $\vec{i} \mapsto \sigma(\vec{i}) = M\vec{i} \mod \vec{b}$  (modulo componentwise). Validity iff  $\vec{i} \bowtie \vec{j}, \vec{i} \neq \vec{j} \Rightarrow \sigma(\vec{i}) \neq \sigma(\vec{j})$  iff, with  $DS = \{\vec{i} - \vec{j} \mid \vec{i} \bowtie \vec{j}\}, DS \cap \ker \sigma = \{\vec{0}\}.$ 

Lattice An allocation is optimal iff its kernel is a strictly admissible (integer) lattice for DS of minimal determinant (critical lattice).



- Successive modulo approach.
- Exhaustive search possible.

• Upper/lower bounds linked to Minkowski's theorems, basis reduction, gauge functions.

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Live-out set of a tiled code:



- Successive modulo:  $(x, y) \mapsto (x \mod N, y \mod N).$
- Skewed mapping:  $(x, y) \mapsto (x - y \mod (2N - 1), y \mod 2).$ 
  - How to find the second one?

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# Many pieces of the puzzle get together

New generalizations and links with previous approaches.

- Liveness analysis for parallel specifications.
- Interference graph structure analysis and exploitation.
- Lattice-based memory allocation extensions.

 Towards a better understanding of parallel languages: semantics, static analysis, and links with the runtime.

And to conclude on tiling:

- Many other extensions exist: tile shapes, parallelism, cost models, etc. See talks by Uday, Sven, Ram.
- Still a need for performance models to guide transformations, parametric tiling is one step. See talk by Markus on perf. models.
- Need to integrate user/algorithm freedom. Ex: domain decomposition to define parallel tiles, multipartitioning for ADI codes, etc.